Fall 2015 EE 491 Weekly Report
Week 11 11/10/2015-11/16/2015

Advisor/Client: Dr. Degang Chen
Members: Yifan Jiang (Webmaster), Scott Poder (Concept Holder), Tao Chen (Team Lead)
Project Title: Low cost high accuracy spectral test system (May1623)

Summary

We discussed the documents and design files which we will need when we hold our electrical design review. We also discussed Timing Diagrams for our ICs, why they are important, how to draft them, and how to create them in simulation. We also clarified that we will be creating a four layer board and will be separating analog and digital components by implementing two separate power planes.

Meeting notes

Time: 10/22/2015 at 1pm **Duration:** 1 hour **Member Present:** All

Purpose and Goals:
Clear up confusion about Timing Diagrams as well as PCB design questions. The goal is to hold our electrical design review the week after Thanksgiving Break.

Achievements:

1. Filter Design Complete - Ran Simulations in TINA-TI
2. Progress on Timing Diagrams
3. Implemented schematic in Multisim
4. Progress is being made on BOM

Pending issues

1. PCB Component Placement/Layout
2. SPI for controlling the chips

Plans for next week

1. Explore connection between FPGA and Test Board
2. Timing Diagram for Relay
3. Controlling the FPGA so that it can do what we plan on it doing for the project

Long Term Goals

1. Schedule Design Review for Week after Thanksgiving Break
2. PCB Fabrication before end of semester

Total contributions

Yifan Jiang: 5 hours: Selected Socket for ADC, FPGA research, SPI issues
Scott Poder: 5 hours: Completed Filter Design and BOM for Filter, Started Timing Diagram Analysis
Tao Chen: 5 hours: Continued progress on PCB Design

This report is created by: Scott Poder on Nov 17