Fall 2015 EE 491 Weekly Report
Week 8 10/20/2015-10/26/2015

Advisor/Client: Dr. Degang Chen
Members: Yifan Jiang (Webmaster), Scott Poder (Concept Holder), Tao Chen (Team Lead)
Project Title: Low cost high accuracy spectral test system(May1623)

Summary

We cleared up additional questions on the Filter Design and the specific frequencies that we will be generating using DAC. We also gave updates on the SPI communication using FPGA and discussed meeting clock generation requirements for different chips.

Meeting notes

Time: 10/22/2015 at 1pm **Duration:** 1 hour **Member Present:** All

Purpose and Goals:
We presented our weekly work to advisor, and we also planned for next week's things to do.

Achievements:

1. Selected DAC8831 as our DAC for sine wave generation
2. Cleared up questions about frequency spacing for RC filter design/relays
3. Design Document V1 created

Pending issues

1. Setting FPGA to generate clocks
2. SPI controlling between chips

Plans for next week

1. Implement Capacitor Bank for RC Filter
2. Implement/Research using a Relay to create different capacitance from Capacitor Bank
3. Implement Power Supply circuit for chips that do not have pre-existing power supplies in the design yet
4. Chip connection and clock for each chip

Total contributions

Yifan Jiang: 8 hours: code for input sine wave, FPGA clock divider design.
Scott Poder: 8 hours: Design Document V1, Continued design on Filters, Relays, and Power Supply Circuits
Tao Chen: 8 hours: Design Document editing, researching on FPGA SPI control on DAC and clock generating.

This report is created by: Scott Poder on Oct 26