Fall 2015 EE 491 Weekly Report
Week 7 10/13/2015-10/19/2015

Advisor/Client: Dr. Degang Chen
Members: Yifan Jiang (Webmaster), Scott Poder (Concept Holder), Tao Chen (Team Lead)
Project Title: Low cost high accuracy spectral test system (May1623)

Summary

We reviewed our design plan, and went through some details. We talked about ADC biasing circuitry, as well as filter designing. And we also decided to use 16-Bits DAC to use for signal generation.

Meeting notes

Time: 10/15/2015 at 1pm **Duration:** 1 hour **Member Present:** All

Purpose and Goals:
We presented our weekly work to advisor, and we also planned for next week's things to do.

Achievements:

1. Confirmed to use LDO for power supply.
2. Clarified that DVDD do not sensitive to noise.
3. LDO power supply for multiple op-amps in the biasing circuits.
4. DAC is chosen as 16-Bits, and sampling rate should higher than ADC's.
5. Filter design methodology was decided.

Pending issues

1. Setting FPGA to generate clocks.
2. SPI controlling between chips.
3. Filter implementation and simulation in the Tina.

Plans for next week

1. Circuit simulation with Tina.
2. DAC choosing on the Ti website.
3. Chip connection and clock for each chip.

Total contributions

Yifan Jiang: 8 hours: Project Plan V1, Researched Filter Design and ROM/DAC sine wave generation
Scott Poder: 8 hours: Project Plan V1, Researched ADC reference and input driver circuit and clock generation
Tao Chen: 8 hours: Project Plan V1, Researched power supply circuits and DAC sine wave generation with SPI

This report is created by: Tao Chen on Oct 19