Fall 2015 EE 491 Weekly Report
Week 5 9/29-10/6/2015

Advisor/Client: Dr. Degang Chen
Members: Yifan Jiang (Webmaster), Scott Poder (Concept Holder), Tao Chen (Team Lead)
Project Title: Low cost high accuracy spectral test system(May1623)

Summary

We reviewed any further questions on Ben's thesis and the circuit design. We cleared up a ton of areas of confusion on the goal of the project, which is to test a large number of identical ADCs of the similar model. We eliminated the microcontroller idea for a sine wave due to too many weaknesses, and set the goal of getting a good start on the circuit schematic before next meeting. We also set deadlines, or milestones, in our project plan.

Meeting notes

Time: 10/1/2015 at 1pm **Duration:** 1 hour **Member Present:** All

Purpose and Goals:

The agenda of this meeting was to clarify questions that originated on the beginning design stages of the circuit schematic regarding the filter design and DAC sine wave generation. We also wanted to clarify that although we have been focusing on the algorithms lately, we should sideline this topic so that we could get a jumpstart on the hardware.

Achievements:

1. Eliminated the microcontroller/sine wave idea due to weakness
2. Cleared up general confusion about the ADCs under test, which will be one model but multiple copies
3. Created version 1 of the project plan and set the schedule with deadlines/milestones
4. Divided up duties for the jumpstart on the schematic design
5. Discussed how the clock frequency of the sine wave generator should be 1/10th the clock of the ADC

Pending issues

1. Confusion about the sampling rate and clock frequency to use for the ADC/Use max? 1MSPS? 80MHz?
2. Idea for using ferrite bead plus capacitors to separate digital and analog supply voltages
3. Question about the mode of the ADC on the digital input: 3wire mode, 4wire mode, daisy chain mode?
4. General FPGA communication and compatibility with design

Plans for next week

1. Get a start on the schematic using TINA CAD software
2. Continue research on filters, FPGA/DAC for sine wave, data output using USB to PC, clock generation
3. Find low dropout regulator chip for 5V (9V battery must drop to 5V to supply for amplifiers)

Total contributions

Yifan Jiang: 8 hours: Project Plan V1, Researched Filter Design and ROM/DAC sine wave generation
Scott Poder: 8 hours: Project Plan V1, Researched ADC reference and input driver circuit and clock generation
Tao Chen: 8 hours: Project Plan V1, Researched power supply circuits and DAC sine wave generation with SPI

This report is created by: Scott Poder on Oct 5