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Introduction

Problem: Accurate Spectral Test is widely used in science and engineering. In particular, accurate spectral test is critical to high performance data converters used in many electronic devices. As a result, there are high standards and requirements on the linearity of the input signals, exact coherency in sampling, and tolerable jitter in the clock signal. As a result, this is very expensive, time consuming, and difficult to maintain and calibrate.

Solution: There are some recently published spectral test algorithms that dramatically relax these stringent requirements of spectral test. We will design a test board for high performance ADCs, implement these algorithms, and compare the accuracy of these results to the traditional test methods.

Design Approach

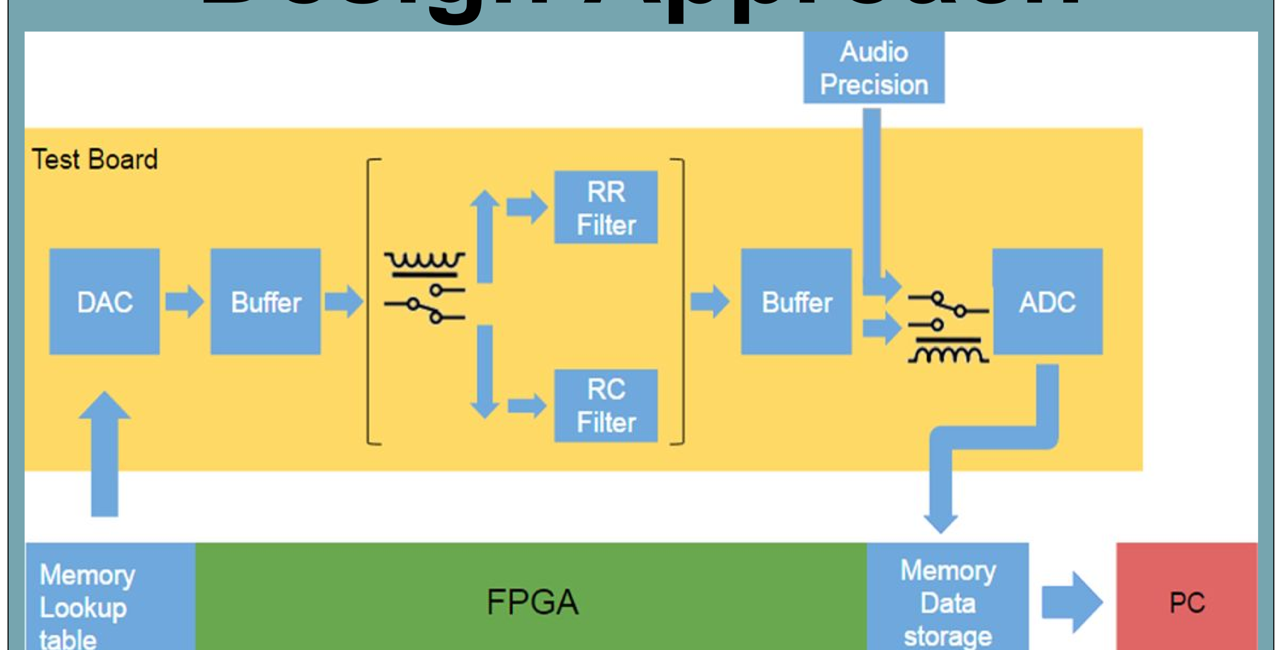
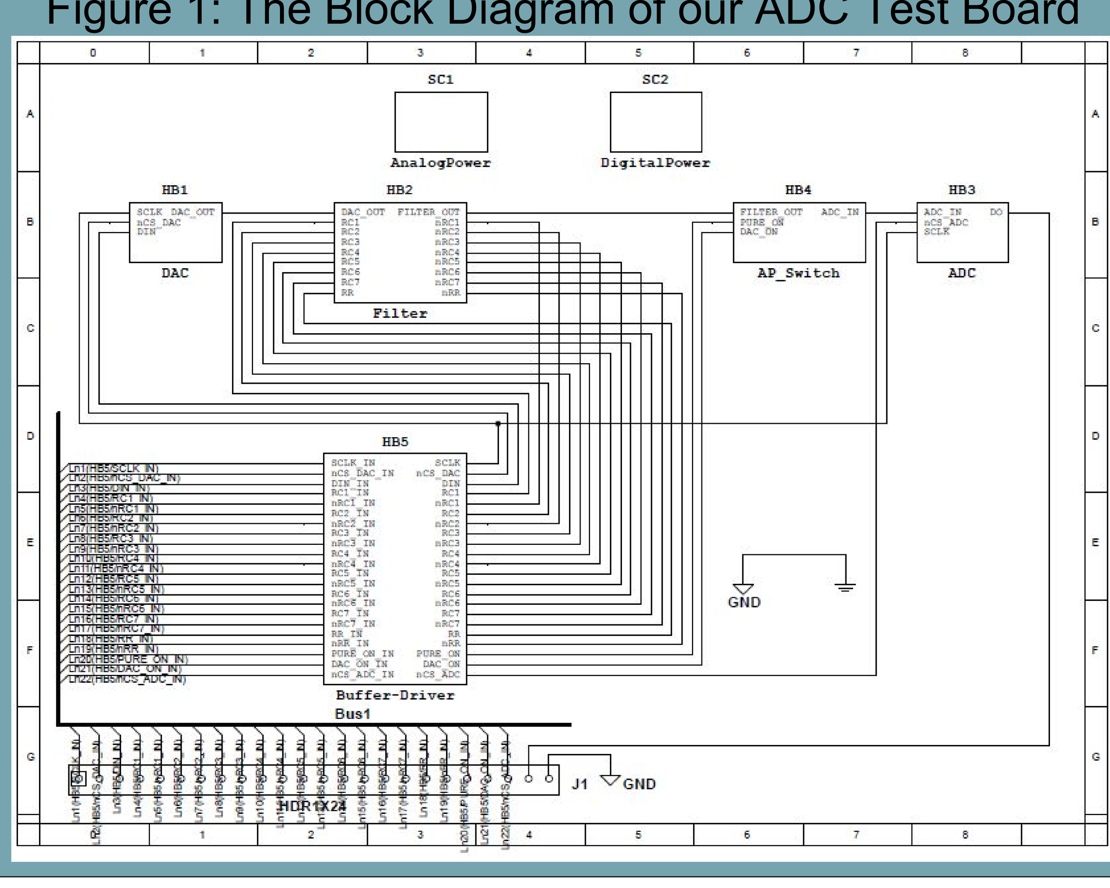


Figure 1: The Block Diagram of our ADC Test Board



Design Requirements

Functional Requirements:

- Deliver Accurate Spectral Test using the new algorithms
  - THD ±1dB compared to Traditional Test Method
- Should not be Time Consuming to obtain results
- Should be completely controllable by the user through a PC
  - Digital Switching in the form of Relays (no physical switches)

Non-Functional Requirements:

- Low Cost in Comparison to the Traditional Spectral Test
  - Traditional Test Method Cost: $28,300
  - New Test Method Cost: Under $500

Operating Environment:

- Test Board
  - Contains DAC, RC and RR Filters, ADC
  - Seen in gold in Figure 1
- FPGA
  - Contains Memory and Clock Generator
  - Seen in green in Figure 1
- PC
  - Contains Verilog code for FPGA and algorithm code in MATLAB

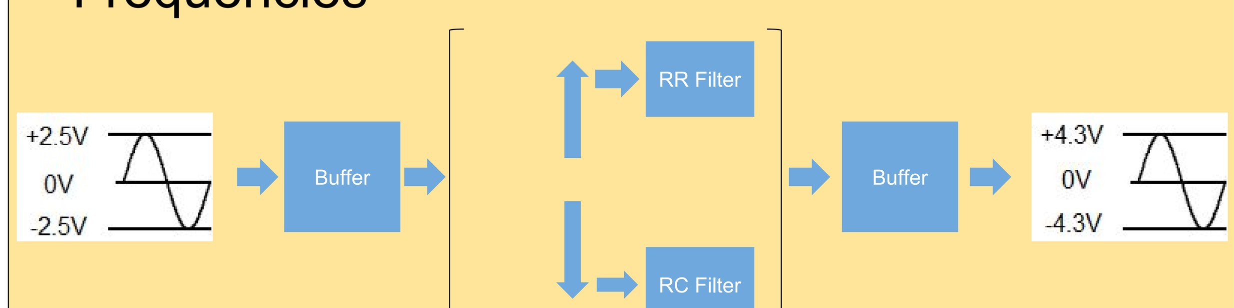
Technical Details Hardware

DAC

- DAC8831 is 16-bit, 2MSPS, and operating in bipolar mode

Filter Design:

- RC Filter - Phase Shift Output
- RR Filter - Match Amplitude of RC Filter
- Input from DAC: ±2.5V sine wave
- Output to ADC: ±4.3V sine wave
  - Gain from Input to Output: 1.72
- RC Filter and RR Filter: sqrt(2) attenuation at -3 dB
  - Adjusted Gain: 1.72*sqrt(2)
- 7 RC Filters + 1RR Filter = 7 Possible Test Frequencies



ADC

- ADC8881 is 18-bit, 1MSPS, and operating in single ended signal configuration

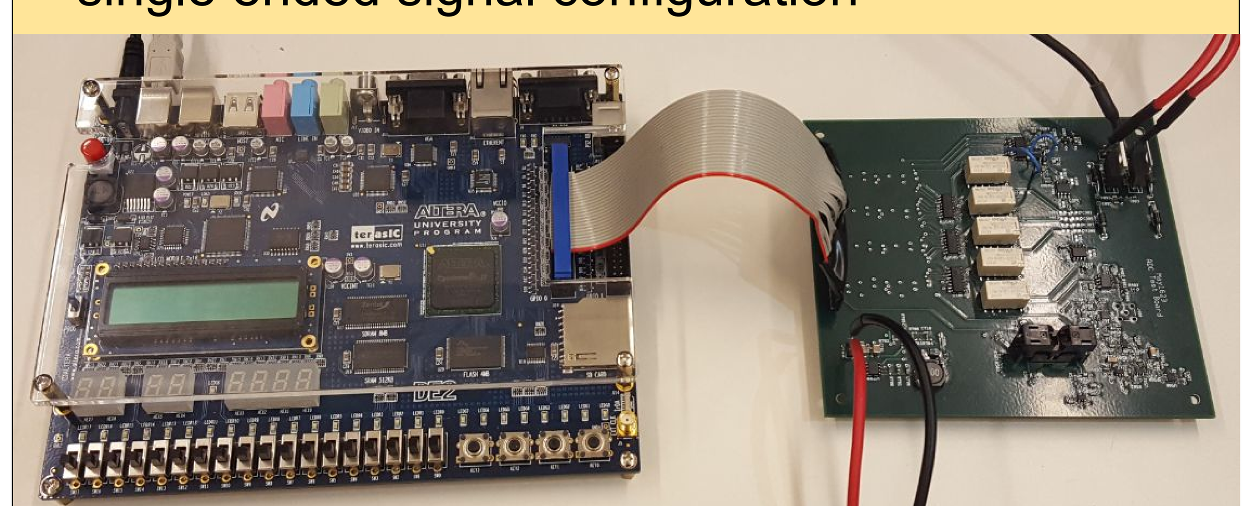


Figure 2: The ADC Test Board (shown left) with the FPGA (shown right)

Technical Details Software

SPI Communication

- 3-Wire Operation for both DAC and ADC
- DAC:CS(chip select), iCLK(clock), SDI(data in)
- ADC:CS(chip select), iCLK, DOUT(data out)

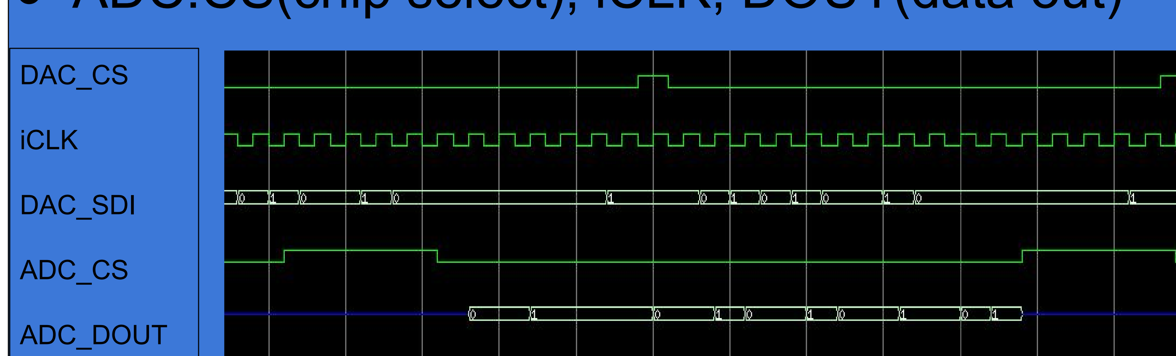


Figure 3: ModelSim Simulation of SPI

Lookup Tables

- 3 Different Tables for different target frequency
- 65536 Numbers within each table
- The range of Table is from 328 to 65208

The left figure seen above shows the general looking of the three lookup table, with frequency equal to 20.3kHz, 13.78kHz and 6.89kHz. The x-axis shows the number of elements in table, and the y-axis tells the values of each elements. The digital number are feeding to DAC in this pattern, to make sure the DAC's outputs are the analog sine wave.

The right figure seen above is the zoom-in version. You can clearly see the three different colors, with different frequency.

Test Results

ADS8881 Testing:

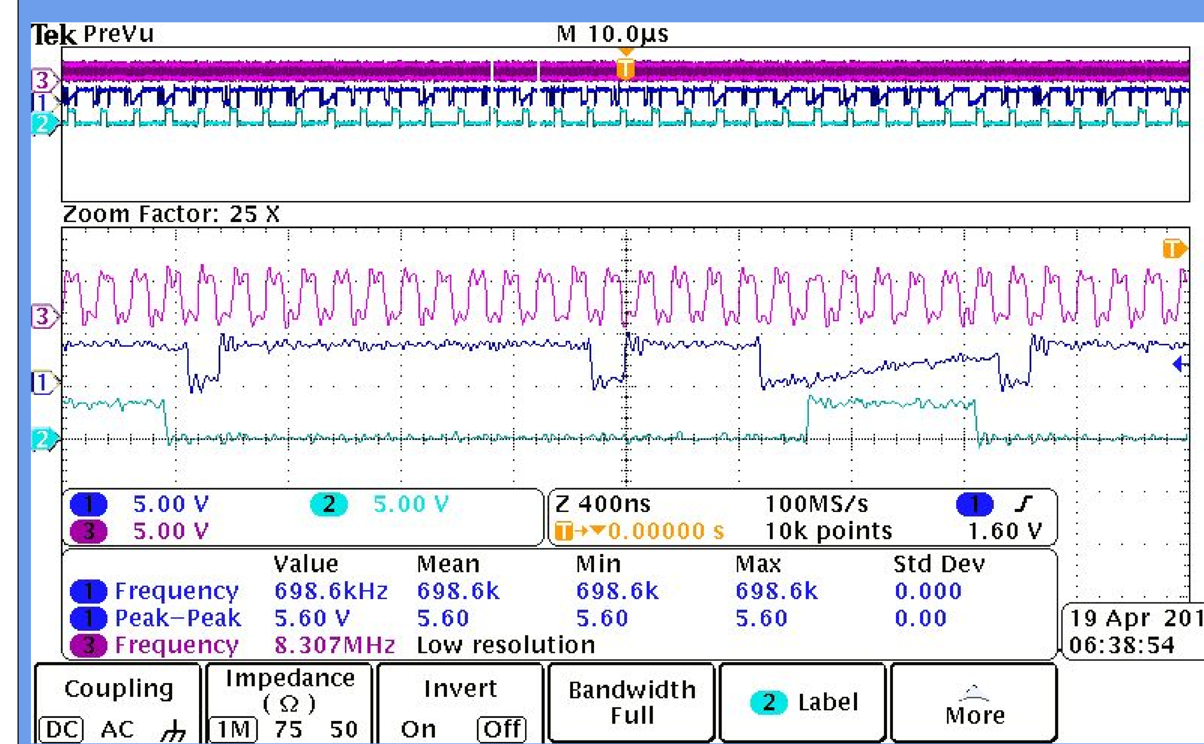


Figure 4: ADC output code for 0V input.

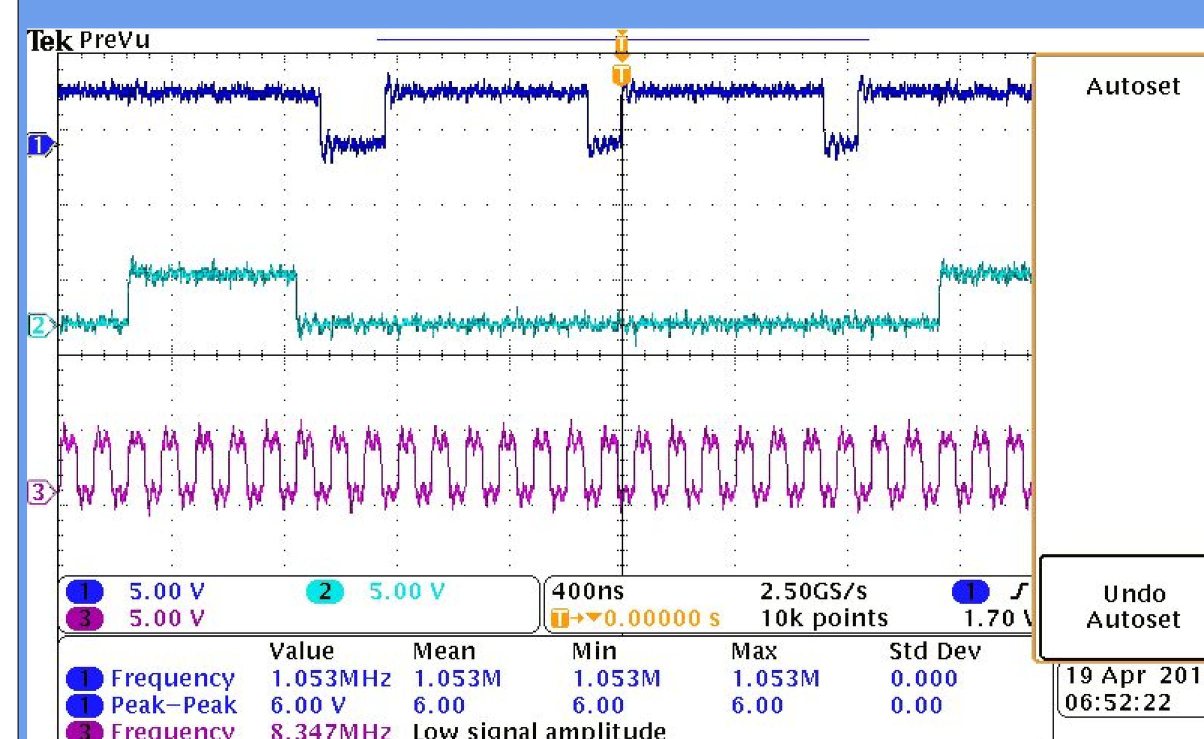


Figure 5: ADC output code for +Vref

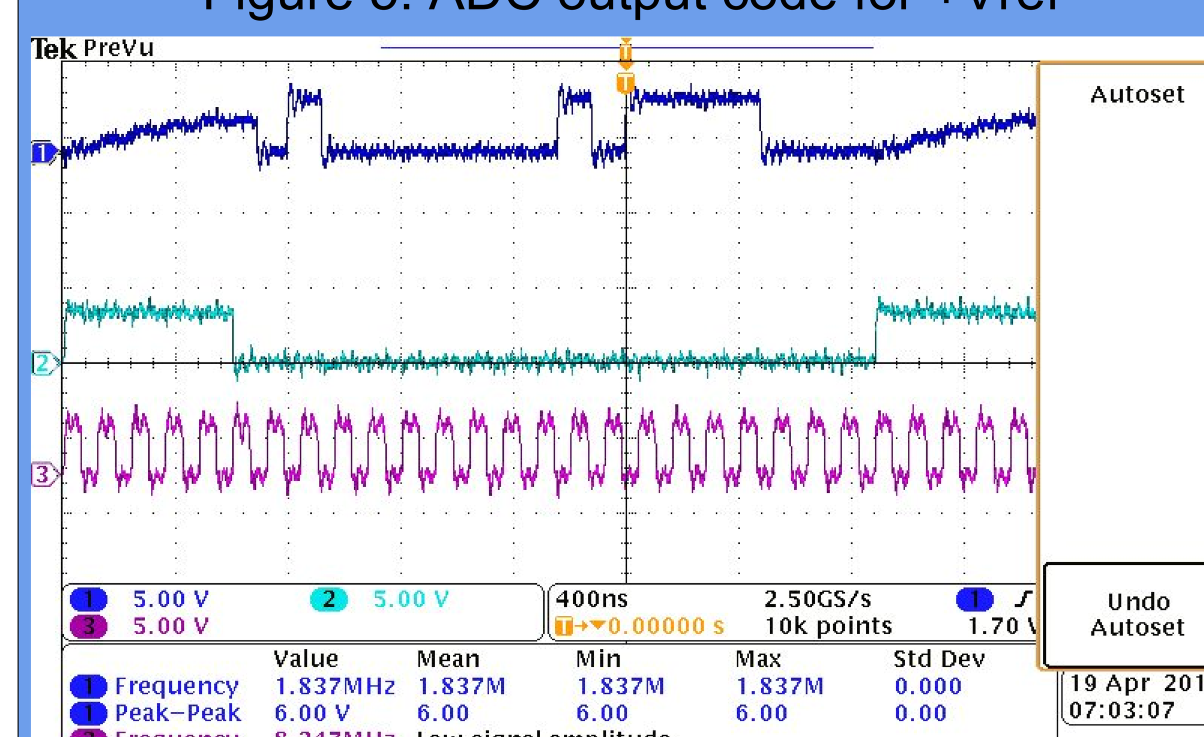


Figure 6: ADC output code for -Vref

Analysis:

- MSB carried out from the falling edge of the chip select, and subsequently
- One Clock Delay Issue for correct results, but if this is taken into account the ADC performs well

Input Voltage	Measured Digital	Expected Digital
0V	11 1111 1111 1011 1100	11 1111 1111 1111 1111
4.5V	01 1111 1011 1111 0111	01 1111 1111 1111 1111
-4.5V	10 0000 0010 1111 0000	10 0000 0000 0000 0000

Future Work

- Future Senior Design Team:
  - Debug ADC Clock Delay Issue
  - Finish Code for Data Collection
  - Perform Spectral Test
    - Compare Traditional vs Nontraditional
  - Create GUI
  - Make Improvements